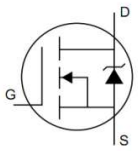
40V N-Channel Power SpeedFET

● General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

● Product Summary



V_{DS}= 40V

$R_{DS(ON)}$ = 2.5mΩ

I_D= 100A

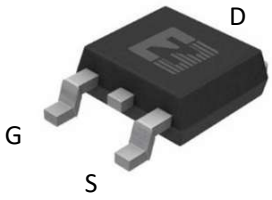
● Features

■AEC-Q101 Qualified

■Low $R_{DS(ON)}$ to minimize conductive loss

■Low Gate Charge for fast switching

■Low Thermal resistance



TO-252

●Application

■BLDC Motor driver

■DC-DC

■Battery protection

●Ordering Information:

Part NO.	ZMSA025N04HD
Marking	ZMS025N04H
Packing Information	REEL TAPE
Basic ordering unit (pcs)	2500

●Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		40	V
Gate-Source Voltage①	V_{GS}		±20	V
Continuous Drain Current	I_D	T_C=25℃	100	A
	I_D	T_C=75℃	91	A
	I_D	T_C=100℃	79	A
Pulsed Drain Current	I_{DM}	Pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C;	400	A
Total Power Dissipation	P_D	T_C=25℃	68	W
Total Power Dissipation	P_D	T_A=25℃	2.4	W
Operating Junction Temperature	T_J		-55 to +175	℃
Storage Temperature	T_{STG}		-55 to +175	℃
Single Pulse Avalanche Energy	E_{AS}	L=0.1mH, V_{GS}=10V, Rg=25Ω,	106	mJ
		L=0.5mH, V_{GS}=10V, Rg=25Ω,	460	mJ
ESD Level (HBM)	CLASS 2			

●Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	2.2	°C/W
Thermal resistance, junction-ambient	R_{thJA} ②		-	62	°C/W
Soldering temperature	Tsold		-	260	°C

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D =250uA	40			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =250uA	2.0	2.7	4.0	V
Drain-Source Leakage Current	I_{DSS}	V_{GS}=0V, V_{DS}= 40V			1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS} = 0V			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D= 40A		2.5	3.2	mΩ
Forward Transconductance	g_{FS}	V_{DS} =5V, I_{SD} = 10A		15		s
Diode Forward Voltage	V_{FSD}	V_{GS} =0V, I_{SD} = 40A			1.3	V

●Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	Ciss	f = 1MHz, V_{DS}=25V	-	2151	-	pF
Output capacitance	Coss		-	578	-	
Reverse transfer capacitance	Crss		-	24	-	
Gate Risistance	Rg	f = 1MHz	-	2.3		Ω
Total gate charge	Qg	V_{DD} = 15V, I_D = 20A, V_{GS} = 10V	-	33	-	nC
Gate - Source charge	Qgs		-	7.6	-	
Gate - Drain charge	Qgd		-	8.3	-	
Turn-ON Delay time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=15V, R_G =3.3Ω, I_D =20A	-	8	-	ns
Turn-ON Rise time	t_r		-	9	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	14	-	ns
Turn-Off Fall time	t_f		-	9	-	ns
Reverse Recovery Time	t_{RR}	V_{DD}=20V, dI_S/dt = 100A/us, I_S=50A	-	35	-	ns
Reverse Recovery Charge	Q_{RR}		-	46	-	nC

Fig.1 Gate-Charge Characteristics

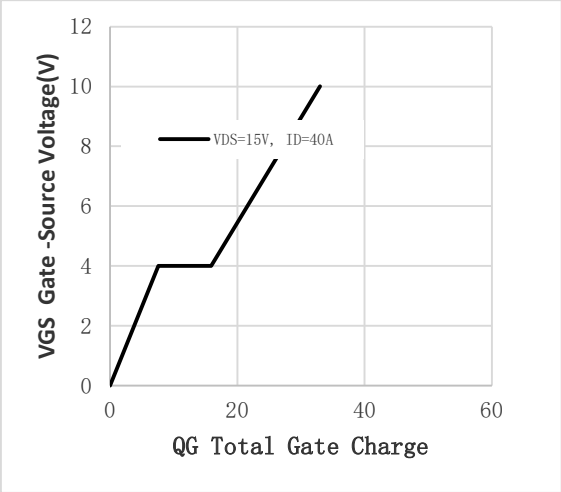


Fig.2 Capacitance Characteristics

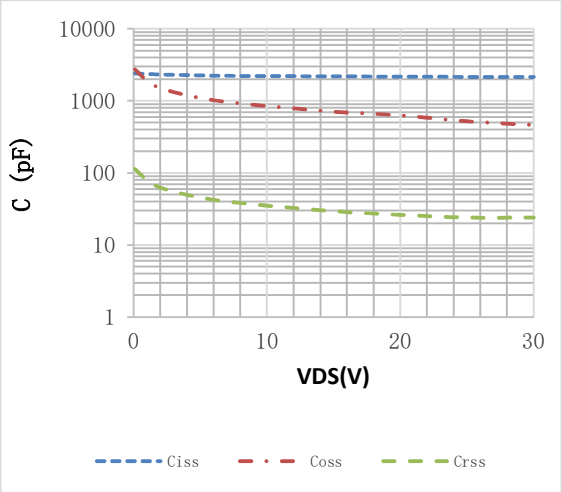


Fig.3 Power Dissipation

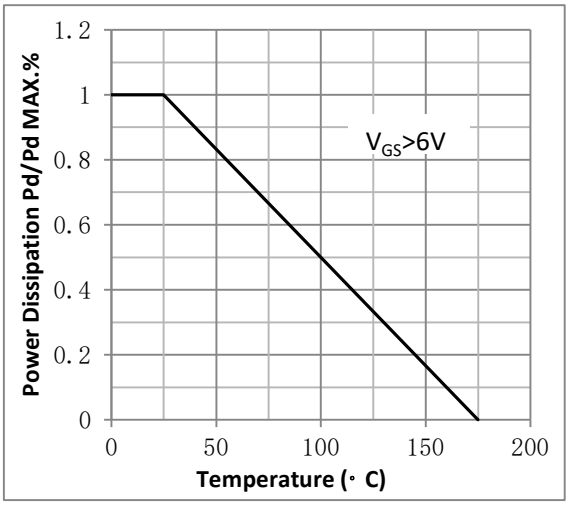


Fig.4 Typical output Characteristics

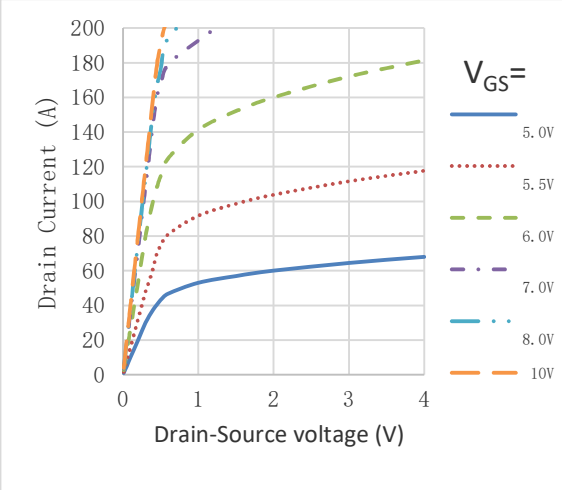


Fig.5 Threshold Voltage V.S Junction Temperature

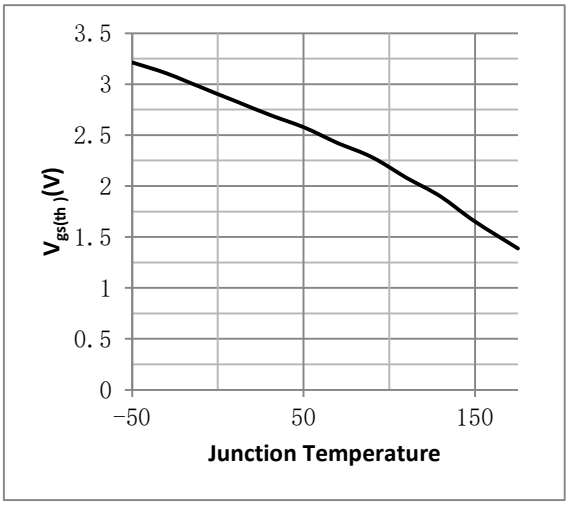


Fig.6 Resistance V.S Drain Current

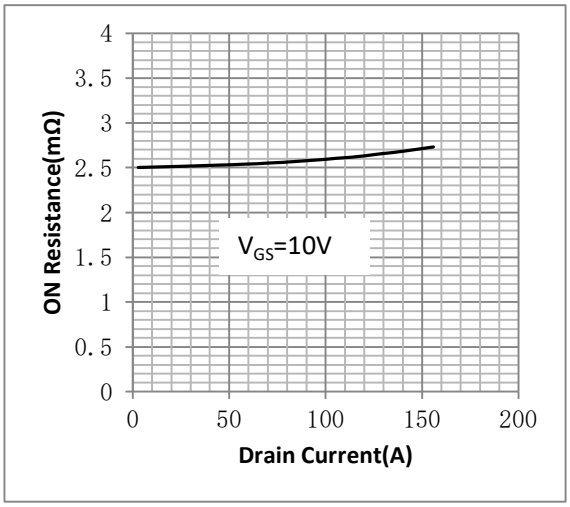


Fig.7 On-Resistance VS Gate Source Voltage

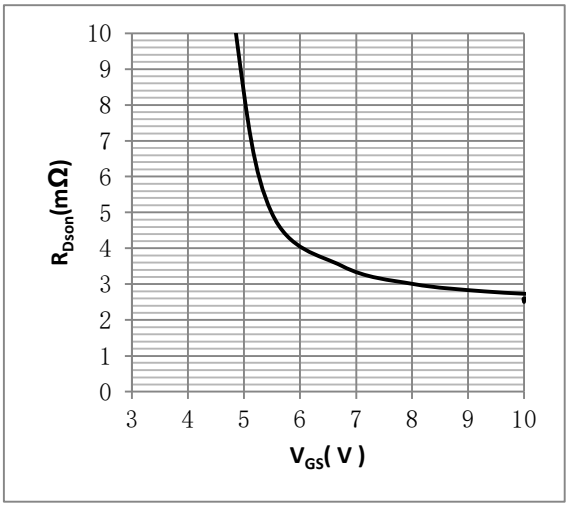


Fig.8 On-Resistance V.S Junction Temperature

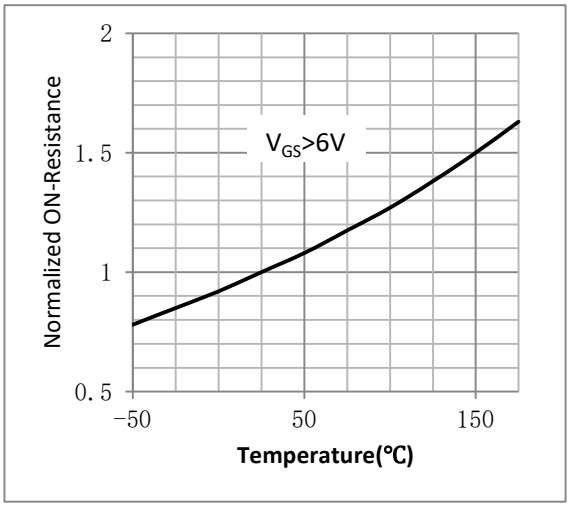


Figure 9. Diode Forward Voltage vs. Current

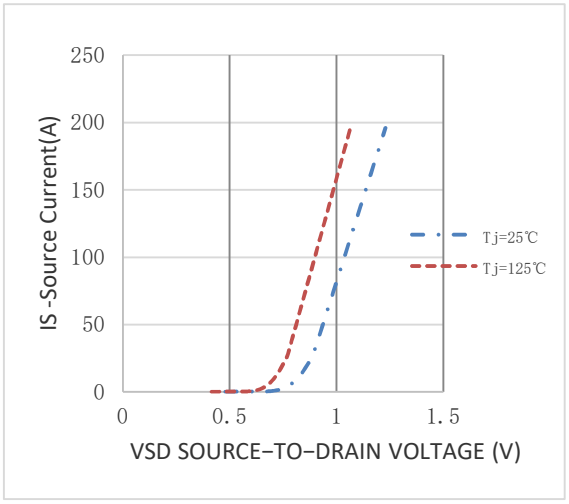


Figure 10. Transfer Characteristics

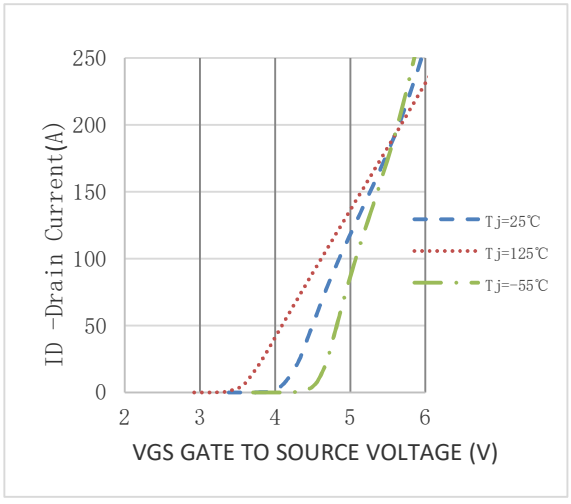


Fig.11 Safe Operating Area

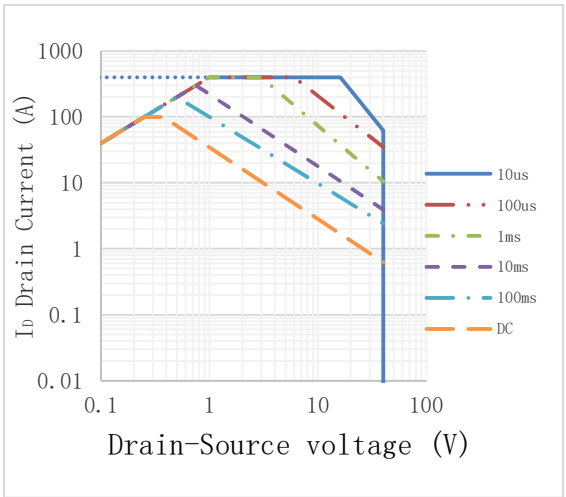
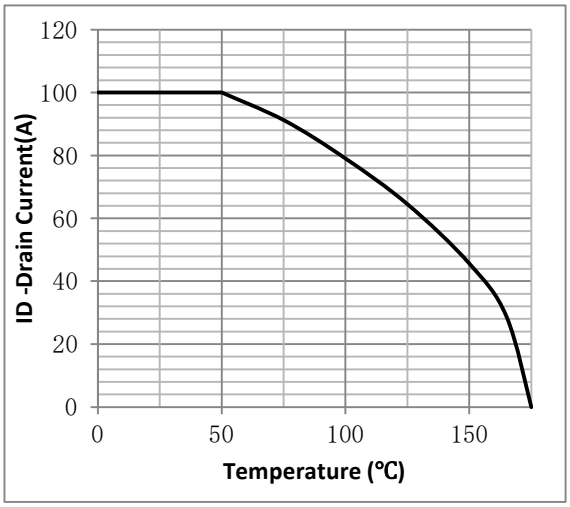
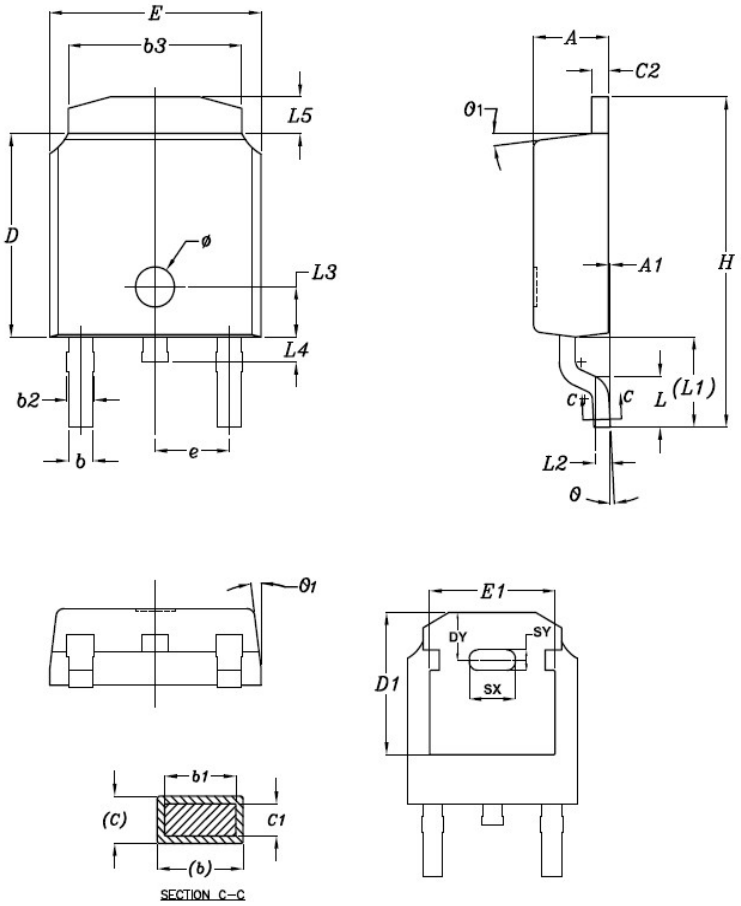


Fig.12 ID vs. Junction Temperature③



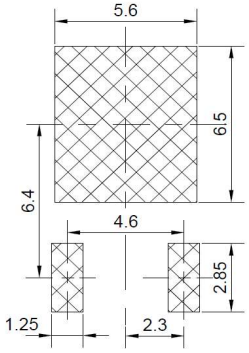
●TO-252 Package Outline

Option Q:



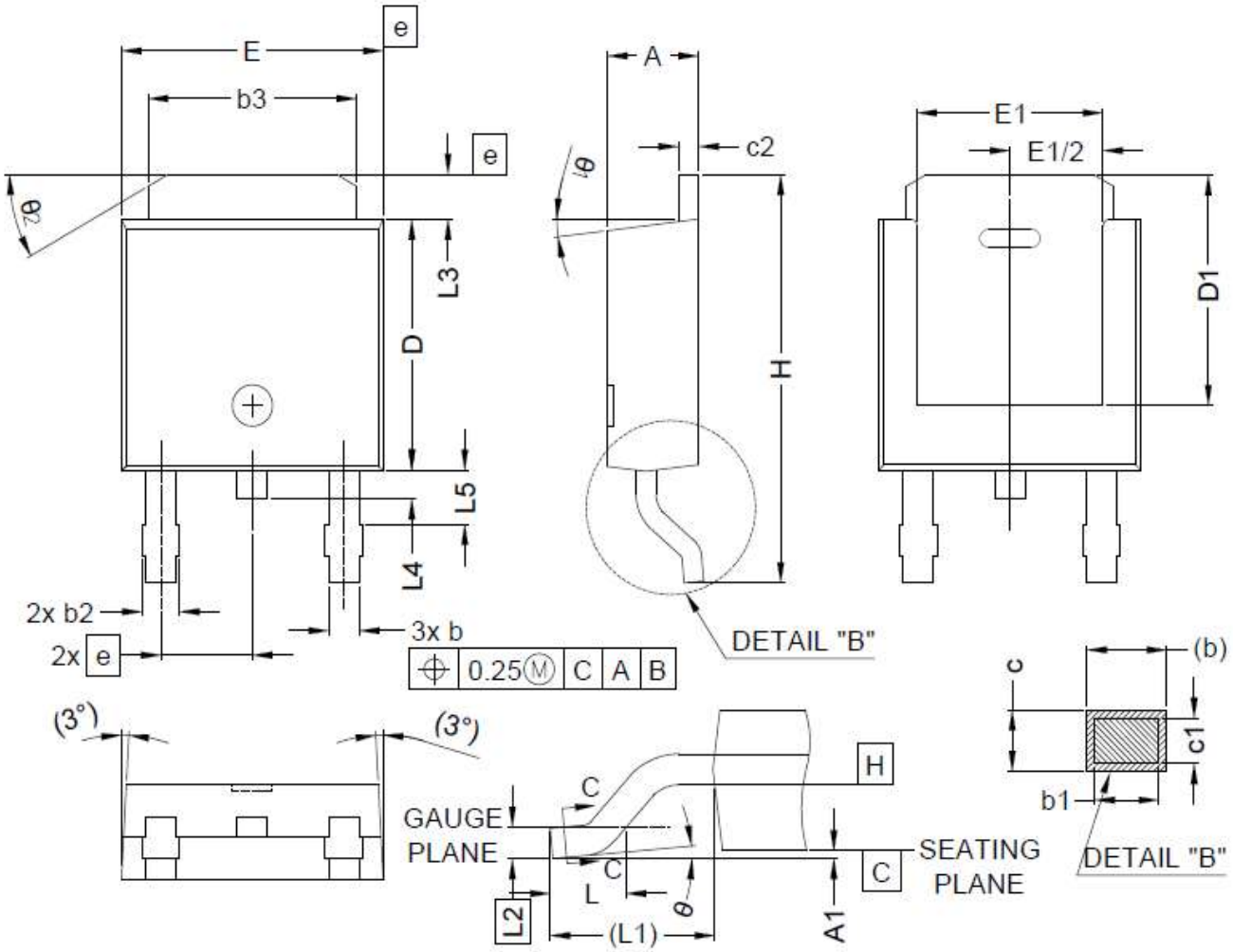
ITEM	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.39	0.086	0.094
A1	——	0.13	——	0.005
b	0.70	0.89	0.028	0.035
b1	0.70	0.86	0.028	0.034
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	5.54	0.205	0.218
E	6.35	6.73	0.250	0.265
E1	4.32	5.27	0.170	0.207
e	2.29 BSC		0.090 BSC	
H	9.40	10.41	0.370	0.410
L	1.40	1.78	0.055	0.070
L1	2.60	2.90	0.102	0.114
L2	0.51 BSC		0.020 BSC	
3 L3	1.65	1.95	0.065	0.077
L4	0.60	0.90	0.024	0.035
3 L5	0.89	1.27	0.035	0.050
θ	1°	5°	1°	5°
θ1	7° REF		7° REF	
ø	1.20 REF		0.047 REF	
SX	1.52 REF		0.060 REF	
SY	0.50 REF		0.020 REF	
DY	1.70 REF		0.067 REF	

Land Pattern
(Only for Reference)



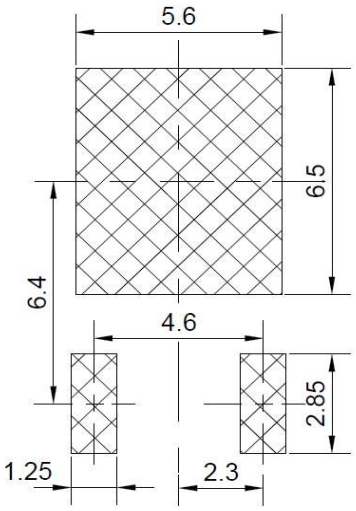
●TO-252 Package Outline

Option A:



SYMBOL	MIN.	MAX.	SYMBOL	MIN.	MAX.	SYMBOL	MIN.	MAX.
A	2.18	2.39	E	6.35	6.73	θ1	0°	15°
A1	-	0.13	E1	4.32	-	θ2	25°	35°
b	0.65	0.89	e	2.29 BSC				
b1	0.64	0.79	H	9.94	10.34			
b2	0.76	1.13	L	1.50	1.78			
b3	4.95	5.46	L1	2.74 REF				
c	0.46	0.61	L2	0.51 BSC				
c1	0.41	0.56	L3	0.89	1.27			
c2	0.46	0.60	L4	-	1.02			
D	5.97	6.22	L5	1.14	1.49			
D1	5.21	-	θ	0°	10°			

Land Pattern
(Only for Reference)



Note:

① Pulse : VGS=+20V/-20V, Duty cycle=50%,Tj=175℃, t=1000 hours; For DC， the following test conditions can be passed: VGS=+20V/-10V, Tj=175℃, t=1000 hours；

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate；

③Practically the current will be limited by PCB, thermal design and operating temperature. V_{GS}=10V.

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Revision History

Version	Date	Change
A	2022.1.6	
B	2022.9.5	1.Add Reach,HF figure,2.ID modify
C	2023.12.19	Correct SOA
D	2025.11.14	Update POD